Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A processor, comprising:

decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode, wherein the decode logic is adapted to switch temporarily or permanently from one mode to another;

pre-decode logic coupled to the decode logic and adapted to operate in parallel with the decode logic; and

wherein the first and second instruction sets each ~~comprises~~ comprise an instruction that temporarily switches the decode logic from one mode to another for at least one subsequent instruction.

2. (Currently Amended) The processor of claim 1, wherein the first and second instruction sets each ~~comprises~~ comprise a Java Impdep1 Bytecode that temporarily switches the decode logic from one mode to another.

3. (Original) The processor of claim 1, wherein the first instruction set comprises a first reserved Java Bytecode that temporarily switches the decode logic from the first mode to the second mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the second instruction set.

4. (Original) The processor of claim 1, wherein the second instruction set comprises a second reserved Java Bytecode that temporarily switches the decode logic from the second mode to the first mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the first instruction set.

5. (Original) The processor of claim 1, wherein the first instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode.

6. (Original) The processor of claim 1, wherein the second instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode.

7. (Original) The processor of claim 6, wherein the instruction that permanently switches the decode logic from the first mode to the second mode succeeds a Java Impdep1 Bytecode.

8. (Original) The processor of claim 1, wherein the second instruction set comprises an instruction that permanently switches the decode logic from the second mode to the first mode.

9. (Currently Amended) A method of decoding instructions from a first and second instruction ~~sets~~set, comprising:

decoding instructions from the first instruction set in a first mode and decoding instructions from a second instruction set in the second mode, wherein the decoding of both instruction sets is performed on a single decoder;

switching the decoding from one mode to another for one instruction; and

switching the decoding permanently from one mode to another.

10. (Original) The method of claim 9, wherein the step of switching the decoding from one mode to another for the one instruction comprises detecting a temporary instruction that indicates the one instruction belongs to another instruction set.

11. (Currently Amended) The method of claim 10, wherein the step of switching the decoding from one mode to another comprises switching from the first mode ~~and~~ to the second mode for the one instruction, wherein the one instruction belongs to the second instruction set.

12. (Currently Amended) The method of claim 10, wherein the step of switching the decoding from one mode to another comprises switching from the second mode ~~and~~ to the first mode for the one instruction, wherein the one instruction belongs to the first instruction set.

13. (Currently Amended) The method of claim 10, wherein the first and second instruction sets each ~~comprises~~ comprise the temporary instruction.

14. (Currently Amended) The method of claim 9, wherein the step of switching the decoding permanently from one mode to another comprises detecting a temporary instruction that indicates the one instruction belongs to another instruction set.

15. (Original) The method of claim 9, wherein the step of switching the decoding permanently from one mode to another further comprises detecting a first permanent instruction that indicates a plurality of instructions belongs to another instruction set.

16. (Original) The method of claim 15, wherein the second instruction set comprises the first permanent instruction.

17. (Original) The method of claim 15, wherein the step of switching the decoding permanently from one mode to another comprises switching the decoding from the first mode to the second mode, wherein the plurality of instructions belong to the second instruction set.

18. (Original) The method of claim 9, wherein the step of switching the decoding permanently from one mode to another comprises detecting a second permanent instruction that indicates a plurality of instructions belongs to another instruction set.

19. (Original) The method of claim 18, wherein the second instruction set comprises the second permanent instruction.

20. (Original) The method of claim 18, wherein the step of switching the decoding permanently from one mode to another comprises switching the second mode to the first mode, wherein the plurality of instructions belong to the first instruction set.

21. (Currently Amended) A processor, comprising:

decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode;

pre-decode logic coupled to the decode logic and adapted to pre-decode instructions in parallel with the decode logic wherein the pre-decode logic pre-decodes for a temporary instruction that switches the decode logic from one mode to another for a subsequent instruction; and

wherein the first and second instruction sets each ~~comprises~~ comprise the temporary instruction and wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

22. (Original) The processor of claim 21, wherein the temporary instruction indicates that the subsequent instruction belongs to another instruction set and causes the decode logic to switch from one mode to another.

23. (Original) The processor of claim 22, wherein the decode logic temporarily switches from the first mode to the second mode, and wherein the subsequent instruction belongs to the second instruction set.

24. (Original) The processor of claim 22, wherein the decode logic temporarily switches from the second mode to the first mode, and wherein the subsequent instruction belongs to the first instruction set.

25. (Original) The processor of claim 21, wherein the subsequent instruction is the first permanent instruction that switches the decode logic permanently from the first the mode to the second mode.

26. (Original) The processor of claim 21, wherein the second permanent instruction permanently switches the decode logic from the second mode to the first mode.

27. (Currently Amended) A system, comprising:

main processor; and

co-processor coupled to the main processor, the co-processor comprising:

decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode;

pre-decode logic coupled to the decode logic and adapted to pre-decode instructions in parallel with the decode logic, wherein the pre-decode logic pre-decodes for a temporary instruction; and

wherein the first and second instruction sets each ~~comprises~~ comprise the temporary instruction, and wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

28. (Original) The system of claim 27, wherein the temporary instruction indicates a subsequent instruction belongs to another instruction set and causes the decode logic to switch from one mode to another.

29. (Original) The system of claim 28, wherein the subsequent instruction belongs to the second instruction set and the decode logic temporarily switches from the first mode to the second mode.

30. (Original) The system of claim 28, wherein the subsequent instruction belongs to the first instruction set and the decode logic temporarily switches from the second mode to the first mode.

31. (Original) The system of claim 28, wherein the subsequent instruction is the first permanent instruction, wherein the first permanent instruction indicates a plurality of instructions from the second instruction set is to follow and permanently switches the decode logic from the first mode to the second mode.

32. (Original) The system of claim 27, wherein the second permanent instruction indicates a plurality of instructions from the first instruction set is to follow and permanently switches the decode logic from the second mode to the first mode.

33. (Original) The system of claim 27, wherein the system comprises a cellular telephone.